REMARKS/ARGUMENTS

Applicants received the Office Action dated March 17, 2004, in which the Examiner: (1) rejected claims 1, 3-8, 10-12, 14-17 and 19-24 as obvious in view of U.S. Pat. App. Pub. No. 20020002262 ("Olarig"), U.S. Patent No. 5,815,457 ("Pascucci") and U.S. Pat. App. Pub. No. 20020161965 ("Ryan"); (2) rejected claims 2, 13 and 18 as obvious in view of Olarig, Pascucci, Ryan and U.S. Pat. App. Pub. No. 20020091905 ("Geiger"); and (3) rejected claim 26 as obvious in view of Olarig, Pascucci, Ryan and U.S. Patent No. 6,275,491 ("Prasad"). In this response, Applicants amend claim 15. Based on the arguments contained herein, Applicants respectfully request reconsideration and allowance of the pending claims.

Rejections Under 35 USC § 103

To reject a claim under 35 USC § 103, the examiner must establish prima facie obviousness. One factor required to establish prima facie obviousness of a claimed invention is that all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). See MPEP 2143.03. Applicant traverses the §103 rejections and respectfully submits that the examiner has not established a prima facie case of obviousness because the cited art does not teach or suggest all the claim limitations.

Claim 1

Claim 1, in part, requires "a first group of bus lines to transfer data bits between a first processing device and a corresponding first memory module" and "a second group of bus lines to transfer data bits between a second processing device and a corresponding second memory module." Claim 1 further requires that "each group of bus lines includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines."

Olarig does not teach "a first processing device and a corresponding first memory module" and "a second processing device and a corresponding second memory module" as suggested by the Examiner (see Office Action, page 2, item 2). Rather, Olarig teaches a heterogeneous memory structure that "allows devices on a processor bus 110a or 110b to access memory modules 320a, despite disparity in type among the memory modules 320a" (see paragraphs [0035-0036]). Olarig does not teach or suggest that devices on the processor bus 110a

or 110b have corresponding memory modules as required of the "first processing device" and the "second processing device" in claim 1. None of the references cited by the Examiner, nor combinations of the references, appears to teach or suggest these limitations.

Further, the Examiner recognizes that Olarig does not teach "each group of bus lines includes two unidirectional bit lines for each data bit" as required in claim 1, but contends that Ryan this limitation. While Ryan teaches a unidirectional command and address (C/A) line, Ryan does not teach or suggest "each group of bus lines includes two unidirectional bit lines for each data bit" as required in claim 1. Specifically, Ryan teaches a "bidirectional data bus for a write operation and receiving information from the bidirectional data bus during a read operation" (see paragraph [0009]). Ryan, therefore, teaches bidirectional data bit lines and not "each group of bus lines includes two unidirectional bit lines for each data bit" as required in claim 1. None of the references cited by the Examiner, nor combinations of the references, appears to teach or suggest this limitation.

The Examiner also recognizes that Olarig does not teach "the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1, but contends that Ryan teaches or suggests this limitation. Applicants, however, cannot find where Ryan teaches or suggests "bus bridges [that] include a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1. The Examiner appears to argue this limitation is suggested by Ryan's "command and address (C/A) buffer register 431 that receives and latches the command and address information from the C/A bus" (see paragraph [0039] and Office Action, page 3, third paragraph). Ryan, however, does not teach or suggest that the C/A buffer register 431 includes "a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner appears to be distilling Applicants' invention down to a "gist" or "thrust" in violation of the requirement to consider the claimed invention as a whole (MPEP 2141.02). None of the references cited by the Examiner, nor combinations of the references, teaches or suggests "a first group of bus lines to transfer data bits between a first processing device and a corresponding first memory module," "a second group of bus lines to transfer data bits between a

second processing device and a corresponding second memory module" and "wherein each group of bus lines includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines" as required in claim 1. For at least the above reasons, individually or in combination, Applicants submit that claim 1 and all claims that depend from claim 1 are allowable.

Claim 11

Claim 11, in part, requires "[a] memory manager setting a router in a conflict-free access pattern in response to said transfer requests" and "the memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses." Claim 11 further requires "local busses [that] each include two unidirectional bit lines for each data bit and [a] cross-bus [that] includes two unidirectional bit lines for each data bit."

The Examiner recognizes that Olarig does not teach "local busses [that] each include two unidirectional bit lines for each data bit" as required in claim 11, but contends that Ryan teaches or suggests this limitation (see Office Action, page 4, last paragraph). As explained previously, Ryan's C/A bus 410 is a unidirectional bus for commands and addresses. The C/A bus 410, therefore, does not teach or suggest "local busses [that] each include two unidirectional bit lines for each data bit" as required in claim 11. Also, Ryan's bidirectional data bus 415 does not teach or suggest "two unidirectional bit lines for each data bit" as required in claim 11. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner appears to be distilling Applicants' invention down to a "gist" or "thrust" in violation of the requirement to consider the claimed invention as a whole (MPEP 2141.02). None of the references cited by the Examiner, nor combinations of the references, teaches or suggests "[a] memory manager setting a router in a conflict-free access pattern in response to said transfer requests," "the memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses" and "the local busses each include two unidirectional bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit" as required in claim 11. For at least the

above reasons, individually or in combination, Applicants submit that claim 11 and all claims that depend from claim 11 are allowable.

Claim 15

Claim 15 was amended to correct a typographical error. Claim 15, in part, requires "a plurality of local bus line groups each for transferring data between a processing device and an associated memory module" and "a memory controller means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules." Claim 15 further requires "the local bus line groups each include oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes oppositely configured unidirectional bit lines for each data bit."

The Examiner recognizes that Olarig does not teach "local bus line groups [that] each include oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes oppositely configured unidirectional bit lines for each data bit" as required in claim 15, but contends that Ryan teaches or suggests this limitation. As explained previously, Ryan teaches a unidirectional command and address (C/A) bus and a bidirectional data bus. However, neither the unidirectional C/A bus nor the bidirectional data bus teaches or suggests "local bus line groups [that] each include oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes oppositely configured unidirectional bit lines for each data bit" as required in claim 15. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

Further, Olarig does not teach or suggest Applicants' claimed "a plurality of local bus line groups each for transferring data between a processing device and an associated memory module" as suggested by the Examiner (see Office Action, page 5). Olarig teaches a heterogeneous memory structure that "allows devices on a processor bus 110a or 110b to access memory modules 320a, despite disparity in type among the memory modules 320a" (see paragraphs [0035-0036]), but does not teach or suggest "local bus line groups each for transferring data between a processing device and an associated memory module" as required in claim 15.

None of the references cited by the Examiner, nor combinations of the references, teaches or suggests this limitation.

Further, Olarig does not teach or suggest Applicants' claimed "the controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" as suggested by the Examiner. As described previously, Olarig does not even teach or suggest "a processing device and an associated memory module" as required in claim 15. While Olarig does mention that "memory requests from a processor have a higher priority than memory requests from other bus masters" (see paragraph [0142]), Olarig still does not teach or suggest "[a] controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" as required in claim 15. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner appears to be distilling Applicants' invention down to a "gist" or "thrust" in violation of the requirement to consider the claimed invention as a whole (MPEP 2141.02). None of the references cited by the Examiner, nor combinations of the references, teaches or suggests "a plurality of local bus line groups each for transferring data between a processing device and an associated memory module," "a memory controller means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" and "the local bus line groups each include oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes oppositely configured unidirectional bit lines for each data bit" as required in claim 15. For at least the above reasons, individually or in combination, Applicants submit that claim 15 is allowable.

Claim 16

Claim 16 requires "a plurality of local memory busses each for transferring data between a processing device and an associated memory module" and "one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection and wherein the local intersect busses are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses." Claim 16 further

requires "a memory controller means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" and "the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each include two unidirectional bit lines for each data bit."

For at least the reasons described previously, with respect to claim 15, Olarig does not teach or suggest "a plurality of local memory busses each for transferring data between a processing device and an associated memory module" nor "the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" as required in claim 16. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

Further, Olarig does not teach or suggest Applicants' claimed "local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection" as suggested by the Examiner (see Office Action, page 7). Olarig teaches a heterogeneous memory structure that allows devices on a processor bus to access memory modules, despite disparity in type among the memory modules. Nothing in Olarig teaches or even suggests "local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection" as required in claim 16. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner recognizes that Olarig does not teach "the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each include two unidirectional bit lines for each data bit" as required in claim 16, but contends that Ryan teaches these limitations. As previously explained, neither the unidirectional C/A bus nor the bidirectional data bus described in Ryan, teaches or suggests "the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each include two unidirectional bit lines for each data bit" as required in claim 16. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner appears to be distilling Applicants' invention down to a "gist" or "thrust" in violation of the requirement to consider the claimed invention as a whole (MPEP 2141.02). None of the references cited by the Examiner, nor combinations of the references, teaches or suggests "a plurality of local memory busses each for transferring data between a processing device and an associated memory module," "one or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection and wherein the local intersect busses are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses," "a memory controller means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules" and "the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each include two unidirectional bit lines for each data bit" as required in claim 16. For at least the above reasons, individually or in combination, Applicants submit that claim 16 and all claims that depend from claim 16 are allowable.

Claim 25

Claim 25 requires "a plurality of memory modules, each memory module being coupled to and paired with one of the processors via separate sets of bus lines such that a data read requested from processor to a paired memory module is received on a first clock cycle subsequent to a clock cycle that provides an address" and "a set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable between the sets of bus lines via the cross-bus lines." Claim 25 further requires that "the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable."

Olarig does not teach Applicants' claimed "a plurality of memory modules, each memory module being coupled to and paired with one of the processors via separate sets of bus lines such that a data read requested from processor to a paired memory module is received on a first clock

cycle subsequent to a clock cycle that provides an address" as suggested by the Examiner (see Office Action, page 9, last paragraph). Nothing in Olarig teaches or even suggests "that a data read requested from processor to a paired memory module is received on a first clock cycle subsequent to a clock cycle that provides an address" as required in claim 25. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

Further, Olarig does not teach Applicants' claimed "set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable between the sets of bus lines via the cross-bus lines" as suggested by the Examiner (see Office Action, page 10). While Olarig teaches "arbitration among multiple memory accesses from multiple sources" (see paragraph [0142]), nothing in Olarig teaches or even suggests "[a] set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable between the sets of bus lines via the cross-bus lines" as required in claim 16. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

Further, Olarig does not teach Applicants' claimed "the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable" as suggested by the Examiner (see Office Action, page 10). Nothing in Olarig teaches or even suggests "the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable" as required in claim 16. None of the references cited by the Examiner, nor combinations of the references, teaches or suggests these limitations.

The Examiner appears to be distilling Applicants' invention down to a "gist" or "thrust" in violation of the requirement to consider the claimed invention as a whole (MPEP 2141.02). None of the references cited by the Examiner, nor combinations of the references, teaches or suggests "a plurality of memory modules, each memory module being coupled to and paired with one of the processors via separate sets of bus lines such that a data read requested from processor to a paired memory module is received on a first clock cycle subsequent to a clock cycle that

provides an address," "a set of segmented cross-bus lines that couple to the separate sets of bus lines using buffers such that multiple data signals are simultaneously transferable between the sets of bus lines via the cross-bus lines" and "cross-bus lines [that] are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable" as required in claim 25. For at least the above reasons, individually or in combination, Applicants submit that claim 25 and all claims that depend from claim 25 are allowable.

CONCLUSION

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

Applicant submits that this response constitutes a complete response to all of the issues raised in the office action of March 17, 2004. Applicants have responded to the various rejections under 35 USC §103. In view of the foregoing amendments and remarks, Applicants submit that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned if a telephone interview might prove helpful in resolving this application.

If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to LSI Logic Corporation Deposit Account Number 12-2252/5201-20400/DJK.

Respectfully submitted,

Daniel J. Krueger
Reg. No. 42,771
Attorney for Applicants
Conley Rose, P.C.
P.O. Box 3267
Houston, Texas 77253-3267
Ph: (713) 238-8000